

1. An integrated circuit package comprising:

- a substrate having a plurality of peripheral openings and first and second surfaces;
- a chip adhered to said second surface of said substrate;
- a plurality of pads disposed on said first surface of said substrate generally centralized within said peripheral openings of said substrate; and
- potting material filling said peripheral openings.

3. The integrated circuit package as recited in claim 1 further comprising a plurality of routing strips being integral with said substrate.

4. The integrated circuit package as recited in claim 3 wherein at least one of said pads disposed on said first

surface of said substrate is electrically connected with at least one of said routing strips.

5 5. The integrated circuit package as recited in claim 1 further comprising at least one solder ball disposed on one of said pads.

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5 6. The integrated circuit package as recited in claim 1 further comprising a plurality of solder balls disposed on said pads forming a high density ball grid array.

7. The integrated circuit package as recited in claim 1 wherein said potting material adheres said chip to said substrate.

8. An integrated circuit package comprising:

a substrate having a plurality of peripheral openings and first and second surfaces;

a plurality of routing strips being integral with said substrate;

a plurality of pads disposed centrally on said first surface, at least one of said pads being electrically connected with at least one of said routing strips;

potting material filling said plurality of peripheral openings;

a chip having a plurality of bonding pads adhered to said second surface of said substrate; and

wire bonding electrically connecting said chip to said substrate between said bonding pads and said routing strips.

9. The integrated circuit package as recited in claim

8 further comprising at least one solder ball disposed on one of said pads.

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10. The integrated circuit package as recited in claim
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8 wherein said at least one solder ball is between about 8 and
20 mils in diameter.

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11. The integrated circuit package as recited in claim
8 further comprising a plurality of solder balls disposed on
said pads forming a high density ball grid array.

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12. The integrated circuit package as recited in claim
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8 wherein said chip has a thickness between about 10 and 20
mils.

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13. The integrated circuit package as recited in claim
a
8 wherein said substrate has a thickness of between about 8
and 28 mils.

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14. The integrated circuit package as recited in claim
a
8 wherein said substrate has first and second layers and
wherein said first layer has a thickness of about 12 mils and
said second layer has a thickness of about 8 mils.

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15. The integrated circuit package as recited in ⁹claim 8
~~claim 8~~
A wherein said substrate has first, second and third layers
A and wherein said first layer has a thickness of about 12 mils,
said second layer has a thickness of about 8 mils and said
5 third layer has a thickness of about 8 mils.

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16. An integrated circuit package comprising:

a substrate having a plurality of peripheral openings,
first and second surfaces and an outline;

a plurality of routing strips being integral with said
substrate;

a plurality of pads centrally disposed on said first
surface at least one of said pads being electrically connected
with said routing strips;

a chip adhered to said second surface of said substrate,
said chip having an outline that is substantially the same as
said outline of said substrate and having a plurality of
bonding pads;

wire bonding electrically connecting said bonding pads to
said routing strips;

vias connecting said routing strips to said pads;

potting material filling said peripheral openings and
covering said wire bonding and said bonding pads; and

a plurality of solder balls centrally disposed on said
pads disposed on said first surface of said substrate forming
a high density ball grid array.

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~~17~~. The integrated circuit package as recited in claim
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~~16~~ wherein said chip has a thickness between about 10 and 20
mils.

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~~18~~. The integrated circuit package as recited in claim
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~~16~~ wherein said substrate has a thickness of between about 8
and 28 mils.

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~~19~~. The integrated circuit package as recited in claim
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~~16~~ wherein said substrate has first and second layers and
wherein said first layer has a thickness of about 12 mils and
said second layer has a thickness of about 8 mils.

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~~20~~. The integrated circuit package as recited in claim
¹⁷
~~16~~ wherein said substrate has first, second and third layers
and wherein said first layer has a thickness of about 12 mils,
said second layer has a thickness of about 8 mils and said
third layer has a thickness of about 8 mils.

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